Exploiting Superword Level Parallelism With Multimedia Instruction Sets

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instructions is the key for performance for many applications. Modern compilers of SIMD instruction sets, once called “multimedia” extensions. Multiple applications benefit from exploiting superword level parallelism within an optimising compiler. Computer architects’ favourite choice of weapon to add to embedded processors is SIMD. ARM offers DSP and multimedia support through their SIMD instruction set. The research paper “Research on Full Length Usage of SIMD Vector Instruction” by Xue and Zhao provides insights into achieving efficient code generation.

In the context of multimedia instruction sets, significant speedup is obtained for the programs that use multimedia and scientific calculations. The increase of vector length and different SIMD instruction sets of SSE, AVX, and Xeon PHI can be exploited to extract superword level parallelism within an optimising compiler. Parallelism with Multimedia Instruction Sets, PowerPoint Presentation, Proceedings of the ACM SIGPLAN Conference, 2000.